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# Description

# METHOD OF FORMING GATE STRUCTURE

## BACKGROUND OF INVENTION

[0001] 1. Field of the Invention

[0002] The present invention relates to a method of forming a gate structure, and more specifically, to a method capable of avoiding word line/bit line short-circuiting.

[0003] 2. Description of the Prior Art

[0004] Dynamic random access memory (DRAM) is composed of many memory cells, and each memory cell has a metal oxide semiconductor (MOS) transistor and a capacitor. The gate of the MOS transistor (also known as word line) serves as a switch of the MOS transistor, while the drain or the source is connected to a bit line for writing and erasing data.

[0005] Please refer and Fig.1 and Fig.2. Fig.1 and Fig.2 are schematic diagrams illustrating a conventional method of forming a gate structure. As shown in Fig.1, primarily, a substrate 10 having at least a stacked gate structure 12 is

provided. The stacked gate structure 12 from bottom to top comprises a gate oxide layer 14, a polysilicon layer 16, a silicide layer 18, and a cap layer 20.

[0006] Then as shown in Fig.2, a chemical vapor deposition (CVD) process is performed to deposit a silicon nitride layer (not shown) onto the substrate 10. Following that, an anisotropic etching process is performed to remove a portion of the silicon nitride layer (not shown) to form a spacer 22 on the sidewalls of the stacked gate structure 12. Finally, an implantation process is performed to form a drain (not shown) and a source (not shown) in the substrate 10.

[0007] The conventional method further comprises the steps of forming a bit line after forming the stacked gate structure 12. Please refer to Fig.3 to Fig.5. Fig.3 to Fig.5 are schematic diagrams showing the steps of forming the bit line. As shown in Fig.3, first a barrier layer 24 is deposited onto the substrate 10 and the stacked gate structure 12. Then a borophosphosilicate glass (BPSG) layer 26 is deposited on the barrier layer 24, and a flow process is performed for planarizing the BPSG layer 26. Finally a chemical mechanical polishing (CMP) process is performed to remove the BPSG layer 26 higher than the cap layer 20.

The material of the barrier layer 24 is silicon nitride, which is capable of preventing the ions of BPSG layer 26 from diffusing into the substrate 10 in the flow process.

[0008] As shown in Fig.4, a dielectric layer 28, such as an oxide layer using TEOS as precursor, is deposited onto the stacked gate structure 12. Then a photo-etching process is performed to remove a portion of the dielectric layer 28, the BPSG layer 26, and the barrier layer 24 for forming a contact hole 30.

[0009] Finally as shown in Fig.5, a bit line 32 is formed for electrically connecting to the drain or source (not shown) of the substrate 10 via the contact hole 30.

[0010] It can be seen from the above description that the conventional method utilizes the spacer 22 to avoid the word line (the polysilicon layer 16 and the silicide layer 18)/bit line short-circuit problem. However, as semiconductor device integrity increases and critical dimension decreases, the spacer 22 is apt to be destroyed in the step of forming the contact hole 30. As shown in Fig.4, the bit line 32 and the silicide layer 18 will be short-circuited easily under this condition. Particularly, when critical dimension is under 0.11μm, the short-circuit problem is not ignorable.

## SUMMARY OF INVENTION

[0011] It is therefore a primary objective of the present invention to provide a method of forming a gate structure capable of solving the above-mentioned problem.

[0012] According to the claimed invention, a method of forming a gate structure is disclosed. First, a substrate is provided, and a gate oxide layer, a polysilicon layer, a silicide layer, and a cap layer are consecutively formed on the substrate. Following that, a portion of the cap layer, the silicide layer, and the polysilicon layer are etched for forming a stacked gate structure. Then, a portion of the silicide layer exposed on sidewalls of the stacked gate structure is removed to form a recess. Finally, a passivation layer is filled into the recess, and the polysilicon layer and the gate oxide layer outside the sidewalls of the stacked gate structure are removed.

[0013] The method of the present invention forms a recess on the sidewalls of the stacked gate structure and fills a passivation layer into the recess so that a word line/bit line short-circuit is avoided. In addition, since the polysilicon layer outside the sidewalls of the stacked gate structure is kept when forming the recess, the gate oxide layer will not be eroded by the etching solution when forming the

recess.

[0014] These and other objects of the present invention will beapparent to those of ordinary skill in the art after having read the following detailed description of the preferred embodiment that is illustrated in the various figures and drawings.

## Brief Description of Drawings

[0015] Fig.1 and Fig.2 are schematic diagrams showing a conventional method of forming a gate structure.

[0016] Fig.3 to Fig.5 are schematic diagrams showing the steps of forming a bit line.

[0017] Fig.6 to Fig.10 are schematic diagrams showing a method of forming a gate structure according to the present invention.

## Detailed Description

[0018] Please refer to Fig.6 to Fig.10, which are schematic diagrams showing a method of forming a gate structure according to the present invention. As shown in Fig.6, first, a substrate 50 is provided, and a gate oxide layer 52, a polysilicon layer 54, a silicide layer 56, a cap layer 58, and a silicon oxynitride layer 60 are consecutively formed on the substrate 50. It is worth noting that in this embodi-

ment of the present invention, the polysilicon layer 54 is doped, and has a thickness of 800Å. The silicide layer 56 is tungsten silicide, and has a thickness of 800 Å. And the cap layer 58 is silicon nitride, and has a thickness of 1600 Å. However, all the above-mentioned materials can be replaced by other materials having similar characteristics, and their thickness are adjustable according to different manufacturing requirements.

[0019] As shown in Fig.7, a photoresist layer (not shown) is coated on the silicon oxynitride layer 60, and an exposure process and a development process are consecutively performed to remove a portion of the photoresist layer (not shown) for forming a photoresist pattern. Then the photoresist pattern 62 is utilized as a hard mask to etch the silicon oxynitride layer 60 not covered by the photoresist pattern 62.

[0020] As shown in Fig.8, first, the photoresist pattern 62 is removed. Then, the remaining silicon oxynitride layer 60 is utilized as a hard mask to etch the cap layer 58, the silicide layer 56, and a portion of the polysilicon layer 54 for forming a stacked gate structure 64.

[0021] As shown in Fig.9, an etching process is then performed by using an ammonium hydrogen peroxide mixture (APM)

solution as an etching solution to remove the silicide layer 56 exposed on the sidewalls of the stacked gate structure 64 such that a recess 66 is formed. The volume ratio of the APM solution is $NH_4OH:H_2O_2:H_2O=1:1:5$ in this embodiment.

[0022] Finally as shown in Fig.10, an etching process is carried out to remove the polysilicon layer 54 and the gate oxide layer 52 not covered by the silicon oxynitride layer 60. Then, a silicon nitride layer 68 is deposited to fill the recess 66. Following this, another etching process is performed to remove the silicon nitride layer 68 outside the recess 66 for accomplishing the stacked gate structure 64. It is worth noting that part of the polysilicon layer 54 is temporarily maintained when forming the recess 66 for protecting the gate oxide layer 52 from being damaged by the APM solution, which will cause the gate oxide layer 52 malfunction. In addition, the silicon nitride layer 68 filled into the recess 66 serves as a passivation layer for avoiding word line/bit line short-circuit in following processes.

[0023] As described in the prior art, steps of forming abit line are followed after the stacked gate structure 64 has to be implemented for forming a complete memory cell. However, since the steps of forming the bit line in the present in-

vention are similar to the steps in the prior art, details are not given again here.

[0024] It is also worth noting that the silicon oxynitride layer 60 serves as a hard mask to form the stacked gate structure 64. Nevertheless, it is not the only way to form the stacked gate structure 64. The cap layer 58 can be also used as a hard mask to form the stacked gate structure 64.

[0025] In comparison with the prior art, the present invention forms a recess in the sidewalls of the stacked gate structure, and fills a passivation layer into the recess for avoiding word line/bit line short-circuit problem. In addition, to prevent the gate oxide layer from being eroded by the etching solution when forming the recess, a portion of the polysilicon layer alongside the sidewalls of the stacked gate structure is temporarily maintained and removed later.

[0026] Those skilled in the art will readily appreciate that numerous modifications and alterations of the device may be made without departing from the scope of the present invention. Accordingly, the above disclosure should be construed as limited only by the metes and bounds of the appended claims.